WHAT IS CLAIMED IS:

1. A ball grid array (BGA) package having a semiconductor chip with edge-bonding metal patterns formed thereon, comprising:

a substrate having circuit patterns for electric connection formed therein;

a center-bonding type semiconductor chip attached to the substrate, the semiconductor chip having center-bonding pads formed on one side thereof;

edge-bonding metal patterns electrically connected to the center-bonding pads of the semiconductor chip, the edge-bonding metal patterns being extended towards the edge regions of the center-bonding type semiconductor chip;

connection members for electrically connecting the edge-bonding metal patterns extended towards the edge regions of the semiconductor chip to the circuit patterns of the substrate, respectively;

a sealing material for molding the substrate to protect the semiconductor chip; and

solder balls attached to solder pads electrically connected to the circuit patterns of the substrate, respectively, for transmitting electric signals from the semiconductor chip to an external substrate.

2. A ball grid array (BGA) package having semiconductor chips with edge-bonding metal patterns formed thereon, comprising:

a substrate having circuit patterns for electric connection formed therein;

a first center-bonding type semiconductor chip attached to the substrate, the first semiconductor chip having center-bonding pads formed on one side thereof;

edge-bonding metal patterns electrically connected to the center-bonding pads of the first semiconductor chip, the edge-bonding metal patterns being extended towards the edge regions of the first center-bonding type semiconductor chip;

a bonding member applied to the first semiconductor chip to form a stacked structure;

a second center-bonding type semiconductor chip stacked on the first semiconductor chip via the bonding member, the second semiconductor chip having center-bonding pads formed on one side thereof;

edge-bonding metal patterns electrically connected to the center-bonding pads of the second semiconductor chip, the edge-bonding metal patterns being extended towards the edge regions of the second center-bonding type semiconductor chip;

connection members for electrically connecting the edge-bonding metal patterns of the first and second semiconductor chips to the circuit patterns of the substrate, respectively;

a sealing material for molding the substrate to protect the first and second semiconductor chips; and

solder balls attached to solder pads electrically connected to the circuit patterns of the substrate, respectively, for transmitting electric signals from the first and second semiconductor chips to an external substrate.

3. The package as set forth in claim 2, wherein the bonding member applied to the first semiconductor chip is a nonconductive bonding agent having spacers therein, the bonding member serving to maintain balance between the first semiconductor chip and the second semiconductor chip and to prevent shorts between the second semiconductor chip and the connection members of the first semiconductor chip.

4. The package as set forth in claim 1 or 2, wherein the metal patterns are formed by means of sputtering a conductive metal.

5. The package as set forth in claim 1 or 2, wherein the connection members are conductive wires.

6. The package as set forth in claim 1, wherein the edge-bonding metal patterns are connected to the corresponding circuit patterns of the substrate at the edge regions of the

semiconductor chip by means of the connection members.

7. The package as set forth in claim 2, wherein the edge-bonding metal patterns are electrically connected to the corresponding circuit patterns of the substrate at the edge regions of the first and second semiconductor chips by means of the connection members, respectively.

8. The package as set forth in claim 1 or 2, wherein the sealing material is synthetic resin.

9. A method of manufacturing a ball grid array (BGA) package having a semiconductor chip with edge-bonding metal patterns formed thereon, comprising the steps of:

carrying out passivation of a wafer having a semiconductor chip with center-bonding pads formed thereon;

forming a stress buffer layer on the wafer to minimize damage to the semiconductor chip;

forming edge-bonding metal patterns on the semiconductor chip to change the center-bonding pads formed on the semiconductor chip into edge-bonding pads in a wafer level;

sawing the wafer having the edge-bonding metal pads formed thereon by units of a prescribed semiconductor chip size;

attaching the semiconductor chip to a substrate by means

of a bonding agent;

electrically connecting the edge-bonding metal patterns formed on the semiconductor chip to circuit patterns formed in the substrate at edge regions of the semiconductor chip by means of connection members, respectively;

molding the substrate with a sealing material to protect the semiconductor chip;

attaching solder balls to solder pads electrically connected to the circuit patterns of the substrate, respectively, so that electric signals from the semiconductor chip are transmitted to an external substrate; and

sawing the substrate having the solder balls attached thereto to obtain a single-layered BGA package.

10. A method of manufacturing a ball grid array (BGA) package having semiconductor chips with edge-bonding metal patterns formed thereon, comprising the steps of:

carrying out passivation of a wafer having a semiconductor chip with center-bonding pads formed thereon;

forming a stress buffer layer on the wafer to minimize damage to the semiconductor chip;

forming edge-bonding metal patterns on the semiconductor chip to change the center-bonding pads formed on the semiconductor chip into edge-bonding pads in a wafer level;

sawing the wafer having the edge-bonding metal pads

formed thereon by units of a prescribed semiconductor chip size;

attaching a first semiconductor chip to a substrate by means of a bonding agent;

electrically connecting edge-bonding metal patterns formed on the first semiconductor chip to circuit patterns formed in the substrate at edge regions of the first semiconductor chip by means of connection members, respectively;

applying a bonding member to the first semiconductor chip to form a stacked structure;

stacking a second semiconductor chip on the first semiconductor chip via the bonding member;

electrically connecting edge-bonding metal patterns formed on the second semiconductor chip to the circuit patterns formed in the substrate at edge regions of the second semiconductor chip by means of connection members, respectively;

molding the substrate with a sealing material to protect the first and second semiconductor chips;

attaching solder balls to solder pads electrically connected to the circuit patterns of the substrate, respectively, so that electric signals from the first and second semiconductor chips are transmitted to an external substrate; and

sawing the substrate having the solder balls attached thereto to obtain a multi-layered BGA package.

11. The method as set forth in claim 9 or 10, wherein the step of forming edge-bonding metal patterns on the semiconductor chip comprises:

coating a photoresist on the stress buffer layer formed on the wafer;

coating a mask having a mask pattern for opening the center-bonding pads of the semiconductor chip on the photoresist;

exposing the stress buffer layer and the photoresist on the unmasked regions;

developing the exposed regions to remove the stress buffer layer and the photoresist so that the center-bonding pads are opened;

exfoliating the photoresist on the masked regions and forming a metal layer to form edge-bonding metal patterns;

coating a photoresist on the metal layer;

coating a mask having a mask pattern for forming edge-bonding metal patterns on the photoresist;

exposing the photoresist on the unmasked regions;

removing the photoresist on the exposed regions and etching the metal layer under the removed photoresist; and

exfoliating the photoresist left on the regions protected

by the mask to form edge-bonding metal patterns on the semiconductor chip.